Title: **METHOD AND STRUCTURE OF DIODE**

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Cross Reference to Related Applications

[0001] This application claims priority of Taiwan Patent Application Serial No. 092103686 filed on February 21, 2003.

Field of Invention

[0002] The present invention relates to a method and a structure of a diode. The diode is used in an electrostatic discharge protection circuit using TFT (thin film transistor) fabrication technology.

Background of the Invention

[0003] There is usually a large amount of charges accumulated in electronic devices (e.g. display panels) during the process of transportation and at various other stages during and after the manufacturing process for such electronic devices. Such accumulation may expose the electronic devices to the impact of a high voltage and cause deteriorated performance or even breakdown of the devices or sometimes even physical injury to the

users. Therefore, it is necessary to install electrostatic discharge (ESD) protection circuits in the electronic devices.

[0004] Fig. 1 shows an electrostatic discharge (ESD) protection circuit **100** adopted in the TFT fabrication process. This protection circuit **100** works through the use of thin film transistors **102, 104** and resistors **106, 108, 109** and **110**. Because of the relative low tolerance of ESD energy for this transistor-resistor arrangement, the electronic discharge protection circuit **100** is not very effective in protecting the electronic devices from ESD.

Summary of the Invention

[0005] The present invention provides a method and a structure of a diode. This diode is used in an electrostatic discharge protection circuit using conventional TFT fabrication technology. This diode can endure a higher ESD energy than the transistor-resistor arrangement previously mentioned and further reduce the possibility of ESD damages on the electronic devices.

[0006] The present invention lies in that the diode is used in an electrostatic discharge protection circuit using TFT fabrication process. Conventional TFT fabrication process can be applied to the fabrication of this diode, and no additional steps or masks are needed. Besides, the carrier concentration modulation is performed in the intrinsic region of the diode, so that the I-V characteristic of the diode is further improved.

[0007] The diode according to the present invention is used as part of an electrostatic discharge protection circuit using TFT fabrication process. The method of fabricating the diode includes the following steps. A semiconductor layer is formed on a substrate. A first region of a first carrier concentration is formed in the semiconductor layer. The first carrier concentration is of a first conductivity type. A second region of a second carrier

concentration is formed in the semiconductor layer. The second carrier concentration is of a second conductivity type. An insulator is formed on the semiconductor layer. The insulator layer is etched to form at least one contact window. The contact window exposes a portion of the upper surface of a semiconductor layer. A metal layer is formed on the insulator layer. The metal layer fills up the contact window to contact the semiconductor layer.

[0008] The first region may be adjacent to the second region in the above-mentioned method or not. Besides, the second conductivity type is a negative type if the first conductivity type is a positive type, while the second conductivity type is a positive type if the first conductivity type is a negative type.

[0009] The above-mentioned method may further include forming a third region in the semiconductor layer before the step of forming the insulator layer. The third region may be intrinsic and located between the first region and the second region. The third region may alternatively be of a third carrier concentration. The third carrier concentration may be of the first conductivity type and may be lower than the first carrier concentration. Then the third region may be located between the first and the second region, and it can be adjacent to the first region.

[0010] The above-mentioned method may further include forming a fourth region in the semiconductor layer before the step of forming the insulator layer. The fourth region may be intrinsic and located between the third region and the second region. The fourth region may alternatively be of a fourth carrier concentration. The fourth carrier concentration may be of the second conductivity type and may be lower than the second carrier concentration. Then the fourth region may be located between the third and the second region, and it can be adjacent to the second region.

[0011] The above-mentioned method may further include forming a fifth region in the semiconductor layer before the step of forming the insulator layer. The fifth region may be intrinsic and located between the third region and the fourth region. The fifth region may alternatively be of a fifth carrier concentration. The fifth carrier concentration may be of the first conductivity type and may be lower than the third carrier concentration. Then the fifth region may be located between the third and the fourth region.

Brief Description of the Drawings

[0012] For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawings. Similar notation number across Figs. 3-8 represents similar element.

[0013] Fig. 1 is a schematic diagram of an electrostatic discharge protection circuit according to the prior art;

[0014] Fig. 2 is a schematic diagram showing an electrostatic discharge protection circuit applying the present invention;

[0015] Fig. 3 is a cross-sectional diagram of a first exemplary embodiment of the present invention;

[0016] Fig. 4 is a cross-sectional diagram of a second exemplary embodiment of the present invention;

[0017] Fig. 5 is a cross-sectional diagram of a third exemplary embodiment of the present invention;

[0018] Fig. 6 is a cross-sectional diagram of a fourth exemplary embodiment of the present invention;

[0019] Fig. 7 is a cross-sectional diagram of a fifth exemplary embodiment of the present invention;

[0020] Fig. 8 is a cross-sectional diagram of a sixth exemplary embodiment of the present invention;

[0021] Fig. 9 is a cross-sectional diagram of a seventh exemplary embodiment of the present invention; and

[0022] Fig. 10 is a cross-sectional diagram of an eighth exemplary embodiment of the present invention.

Detailed Description

[0023] Fig. 2 is a schematic diagram showing an embodiment of the electrostatic discharge protection circuit **200** applying the present invention. The diodes **204, 206, 208** and **210** according to the present invention are located among the internal circuit **202,** VDD, and VSS to achieve protection. The carrier concentration modulation is performed in the intrinsic region of the diodes **204, 206, 208** and **210**. The diodes **204, 206, 208** and **210** may utilize different carrier concentration to improve characteristic of endure high ESD energy.

[0024] Fig. 3 is a cross-sectional diagram of the first exemplary embodiment **300** of the present invention. This exemplary embodiment **300** includes a semiconductor layer **304**, an insulator layer **310** and a metal layer **314**. The semiconductor layer **304** includes a first region **306** of a first carrier concentration and a second region **308** of a second carrier concentration. The insulator layer **310** is disposed on the semiconductor layer **304** and includes at least one contact window **312**. The metal layer **314** is disposed on the insulator layer **310**. The contact window **312** exposes a portion of the upper surface of the semiconductor layer **304**. The metal layer **314** fills up the contact window **312** to contact the semiconductor layer **304**. The first carrier concentration is of the positive conductivity

type. The second carrier concentration is of the negative conductivity type. The first region **306** is adjacent to the second region **308**.

[0025] Fig. 4 is a cross-sectional diagram of the second exemplary embodiment **400** of the present invention. The semiconductor layer **304** of this exemplary embodiment **400** includes a first region **406** of a first carrier concentration and a second region **408** of a second carrier concentration. The first carrier concentration is of the positive conductivity type. The second carrier concentration is of the negative conductivity type. The first region **406** is not adjacent to the second region **408**. A third region **416** is located between the first region **406** and the second region **408**. In this exemplary embodiment **400**, the third region **416** is intrinsic.

[0026] Fig. 5 is a cross-sectional diagram of the third exemplary embodiment **500** of the present invention. The semiconductor layer **304** of this exemplary embodiment **500** includes a first region **506** of a first carrier concentration, a second region **508** of a second carrier concentration and a third region **516** of a third carrier concentration. The first carrier concentration is of the positive conductivity type. The second carrier concentration is of the negative conductivity type. The third carrier concentration is of the positive conductivity type and is lower than the first carrier concentration. The third region **516** is located between the first region **506** and the second region **508**, and is respectively adjacent to the first region **506** and the second region **508**.

[0027] Fig. 6 is a cross-sectional diagram of the fourth exemplary embodiment **600** of the present invention. The semiconductor layer **304** of this exemplary embodiment **600** includes a first region **606** of a first carrier concentration, a second region **608** of a second carrier concentration and a third region **616** of a third carrier concentration. The first carrier concentration is of the positive conductivity type. The second carrier concentration is of the negative conductivity type. The third carrier concentration is of the negative

conductivity type and is lower than the second carrier concentration. The third region **616** is located between the first region **606** and the second region **608**, and is respectively adjacent to the first region **606** and the second region **608**.

[0028] Fig. 7 is a cross-sectional diagram of the fifth exemplary embodiment **700** of the present invention. The semiconductor layer **304** of this exemplary embodiment **700** includes a first region **706** of a first carrier concentration, a second region **708** of a second carrier concentration, a third region **716** of a third carrier concentration and a fourth region **718** of a fourth carrier concentration. The first carrier concentration is of the positive conductivity type. The second carrier concentration is of the negative conductivity type. The third carrier concentration is of the positive conductivity type and is lower than the first carrier concentration. The fourth carrier concentration is of the negative conductivity type and is lower than the second carrier concentration. Both the third region **716** and the fourth region **718** are located between the first region **706** and the second region **708**. The third region **716** is adjacent to the first region **706**. The fourth region **718** is adjacent to the second region **708**. The third region **716** is adjacent to the fourth region **718**.

[0029] Fig. 8 is a cross-sectional diagram of the sixth exemplary embodiment **800** of the present invention. This exemplary embodiment **800** is similar to the fifth exemplary embodiment **700**, while the difference between the embodiments **700** and **800** lies in that the fourth region **818** is intrinsic.

[0030] Fig. 9 is a cross-sectional diagram of the seventh exemplary embodiment **900** of the present invention. This exemplary embodiment **900** is similar to the fifth exemplary embodiment **700**, while the difference between the embodiments **700** and **900** lies in that the third region **916** is intrinsic.

[0031] Fig. 10 is a cross-sectional diagram of the eighth exemplary embodiment **1000** of the present invention. The semiconductor layer **304** of this exemplary embodiment **1000**

includes a first region **1006** of a first carrier concentration, a second region **1008** of a second carrier concentration, a third region **1016** of a third carrier concentration, a fourth region **1018** of a fourth carrier concentration and a fifth region **1020**. The first carrier concentration is of the positive conductivity type. The second carrier concentration is of the negative conductivity type. The third carrier concentration is of the positive conductivity type and is lower than the first carrier concentration. The fourth carrier concentration is of the negative conductivity type and smaller than the second carrier concentration. Both the third region **1016** and the fourth region **1018** are located between the first region **1006** and the second region **1008**. The third region **1016** is adjacent to the first region **1006**. The fourth region **1018** is adjacent to the second region **1008**. The third region **1016** is not adjacent to the fourth region **1018**. The fifth region **1020** is located between the third region **1016** and the fourth region **1018**. The fifth region **1020** is intrinsic in this embodiment **1000**. However, the fifth region **1020** may alternatively be of a fifth carrier concentration. The fifth carrier concentration may be of the positive conductivity type and is lower than the third carrier concentration. The fifth carrier concentration may alternatively be of the negative conductivity type and is lower than the fourth carrier concentration.

[0032] While this invention has been described with reference to the illustrative embodiments, these descriptions should not be construed in a limiting sense. Various modifications of the illustrative embodiment, as well as other embodiments of the invention, will be apparent upon reference to these descriptions. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as falling within the true scope of the invention and its legal equivalents.